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<b>(21) International Application Number:</b> PCT/US99/11171 <b>(22) International Filing Date:</b> 19 May 1999 (19.05.99) <b>(30) Priority Data:</b> 60/087,206 28 May 1998 (28.05.98) US <b>(63) Related by Continuation (CON) or Continuation-in-Part (CIP) to Earlier Application</b> US Not furnished (CON) Filed on 19 May 1999 (19.05.99) <b>(71) Applicant (for all designated States except US):</b> TECSTAR POWER SYSTEMS, INC. [US/US]; 15251 Don Julian Road, City of Industry, CA 91745 (US). <b>(72) Inventors; and</b> <b>(75) Inventors/Applicants (for US only):</b> HO, Frank [US/US]; 5644 Calle Vista Alegre, Yorba Linda, CA 92887 (US). YEH, Milton, Y. [US/US]; 1454 Princeton Street, Santa Monica, CA 90404 (US). CHU, Chaw-Long [US/US]; 1436 Rancho Hills Drive, Chino Hills, CA 91709 (US). ILES, Peter, A. [US/US]; 1000 Park Avenue, Arcadia, CA 91007 (US).		<b>(74) Agent:</b> ALTMAN, Daniel, E.; Knobbe, Martens, Olson & Bear, LLP, 16th floor, 620 Newport Center Drive, Newport Beach, CA 92660 (US). <b>(81) Designated States:</b> AE, AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).  <b>Published</b> <i>With international search report.</i>
<b>(54) Title: SOLAR CELL HAVING AN INTEGRAL MONOLITHICALLY GROWN BYPASS DIODE</b>		
<b>(57) Abstract</b>		
<p>The present invention is directed to systems and methods for protecting a solar cell. The solar cell includes first solar cell portion. The first solar cell portion includes at least one junction and at least one solar cell contact on a backside of the first solar cell portion. At least one bypass diode portion is epitaxially grown on the first solar cell portion. The bypass diode has at least one contact. An interconnect couples the solar cell contact to the diode contact.</p>		

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**SOLAR CELL HAVING AN INTEGRAL MONOLITHICALLY GROWN BYPASS DIODE****Background Of The Invention****Field Of The Invention**

The present invention relates to solar cells. In particular, the present invention relates to methods and apparatuses for providing a solar cell with an integral diode.

**Description Of The Related Art**

Photovoltaic cells, commonly called solar cells, are well-known devices which convert solar energy into electrical energy. Solar cells have long been used to generate electrical power in both terrestrial and space applications. Solar cells offer several advantages over more conventional power sources. For example, solar cells offer a clean method for generating electricity. Furthermore, solar cells do not have to be replenished with fossil fuels. Instead, solar cells are powered by the virtually limitless energy of the sun. However, the use of solar cells has been limited because solar cells are a relatively expensive method of generating electricity. Nonetheless, the solar cell is an attractive device for generating energy in space, where low-cost conventional power sources are unavailable.

Solar cells are typically assembled into arrays of solar cells connected together in series, or in parallel, or in a series-parallel combination. The desired output voltage and current, at least in part, determine the number of cells in an array, as well as the array topology.

As is well known in the art, when all cells in an array are illuminated, each cell will be forward biased. However, if one or more of the cells is shadowed (i.e., not illuminated), by a satellite antenna or the like, the shadowed cell or cells may become reversed biased because of the voltage generated by the unshadowed cells. Reverse biasing of a cell can cause permanent degradation in cell performance or even complete cell failure. To guard against such damage, it is customary to provide protective bypass diodes. One bypass diode may be connected across several cells, or for enhanced reliability, each cell may have its own bypass diode. Multijunction solar cells are particularly susceptible to damage when subjected to a reverse bias condition. Thus, multijunction cells in particular benefit from having one bypass diode per cell. Conventionally, a bypass diode is connected in an anti-parallel configuration, with the anode and the cathode of the bypass diode respectively connected to the cathode and the anode of the solar cell, so that the bypass diode will be reversed biased when the cells are illuminated. When a cell is shadowed, current through the shadowed cell becomes limited and the shadowed cell becomes reverse biased. The bypass diode connected across the shadowed cell in turn becomes forward biased. Most of the current will flow through the bypass diode rather than through the shadowed cell, thereby allowing current to continue flowing through the array. In addition, the bypass diode limits the reverse bias voltage across the shadowed cell, thereby protecting the shadowed cell.

Several different conventional methods have been used to provide solar cells with bypass diode protection. Each conventional method has its drawbacks. For example, in an attempt to provide increased bypass protection, one method involves locating a bypass diode between adjacent cells, with the anode of the bypass diode connected to one cell and the cathode of the diode connected to an adjoining cell. However, this technique requires that the cells be assembled into an array before the bypass diode protection can be added. This assembly method is difficult and

inefficient. Furthermore, this technique requires the bypass diodes to be added by the array assembler, rather than the cell manufacturer. In addition, this technique requires the cells to be spaced far enough apart so as to accommodate the bypass diode. This spacing results in the array having a lower packing factor, and thus, the array is less efficient on an area basis.

5 Another conventional technique providing a bypass diode for each cell requires that a recess be formed on the back of the cell in which a bypass diode is placed. Each cell is provided with a first polarity contact on a front surface of the cell and a second polarity contact is provided on a back surface of each cell. An "S" shaped interconnect must then be welded from a back surface contact of a first cell to a front surface contact of an adjoining cell. Thus, this technique disadvantageously requires the cells to be spaced far enough apart to accommodate the interconnect which  
10 must pass between the adjoining cells. Additional disadvantages of this method include the possibility of microcracks generated during formation of the recess. In addition, this technique requires a thick bondline of adhesive, thereby adding stress-risers, increasing stresses generated during temperature cycling. Furthermore, the present conventional technique requires the connection of the interconnect to the adjoining cell to be performed by the array assembler as opposed to the cell manufacturer.

#### 15 Summary of the Invention

One embodiment of the present invention advantageously provides methods and systems for efficiently providing an integral bypass diode on a solar cell. In one embodiment, the solar cell is a multijunction cell. The bypass diode is monolithically grown over at least a portion of the solar cell. In another embodiment, the solar cell is formed from at least group III, IV, or V materials. In still another embodiment, the diode includes at least an N-type GaAs layer  
20 and a P-type GaAs layer. In yet another embodiment, the diode is formed using lower bandgap materials, such as germanium or InGaAs.

In one embodiment, the solar cell includes a germanium Ge substrate. The Ge substrate may further include a photoactive junction. In yet another embodiment, the substrate is formed from at least one of the following materials: semiconductors, such as GaAs, Si, or InP, and insulators, such as sapphire. In one embodiment, the substrate is a  
25 single crystal.

In yet another embodiment, a C-clamp conductor interconnects at least one solar cell contact to at least one bypass diode contact. In another embodiment, an integrally metallized layer is used to interconnect at least one solar cell contact to at least one bypass diode contact. In still another embodiment, the integrally metallized layer is deposited over an insulating layer to prevent the integrally metallized layer from shorting to one or more other layers.

30 In one embodiment, a cap layer interconnects a first diode polarity with the solar cell. In yet another embodiment, the bypass diode is epitaxially grown on a solar cell having one or more junctions. In still another embodiment, the solar cell may be formed from at least one or more of the following materials: GaAs, InP, GaInP<sub>2</sub>, and AlGaAs. In another embodiment, other III-V compounds are used to form at least a portion of the solar cell.

**Brief Description of the Drawings**

These and other aspects, advantages, and novel features of the invention will become apparent upon reading the following detailed description and upon reference to accompanying drawings in which:

- Figure 1 illustrates a first processing step used to construct one embodiment of the present invention;
- 5 Figure 2 illustrates a second processing step used to construct one embodiment of the present invention;
- Figure 3 illustrates a third processing step used to construct one embodiment of the present invention;
- Figure 4 illustrates a fourth processing step used to construct one embodiment of the present invention;
- Figure 5 illustrates a fifth processing step used to construct one embodiment of the present invention;
- Figure 6 illustrates a sixth processing step used to construct one embodiment of the present invention;
- 10 Figure 7 illustrates a seventh processing step used to construct one embodiment of the present invention;
- Figure 8 illustrates an eighth processing step used to construct one embodiment of the present invention;
- Figure 9 illustrates a ninth processing step used to construct one embodiment of the present invention;
- Figure 10 illustrates a tenth processing step used to construct one embodiment of the present invention;
- Figure 11 illustrates one embodiment of the present invention, including a discrete interconnect;
- 15 Figure 12 illustrates one embodiment of the present invention, including an integral interconnect;
- Figure 13A illustrates a perspective view of one embodiment of the present invention;
- Figure 13B illustrates in greater detail the bypass diode illustrated in Figure 13A.
- Figure 14A illustrates one embodiment of the present invention with a buried bypass diode;
- Figure 14B illustrates the embodiment of Figure 14A after further processing acts are performed;
- 20 Figure 15A illustrates a first method of interconnecting solar cells; and
- Figure 15B illustrates a second method of interconnecting solar cells.

**Detailed Description of the Preferred Embodiments**

The present invention relates to a solar cell with at least one integral bypass diode. The solar cell may be a single junction or multijunction cell. As discussed below, in one embodiment, a bypass diode is epitaxially grown on a multijunction solar cell. The solar cell/bypass diode device may be interconnected with other solar cells to form series and/or parallel strings of solar cells. The strings may be further connected to form a reliable and robust solar cell array. The solar cell array may be mounted to a space vehicle, thereby providing power to the space vehicle.

Figure 1 shows a sequence of III-V layers 106-122 which are grown sequentially on a Ge substrate 102 in one embodiment of the present invention to form a multijunction solar cell 100. The Ge substrate 102 may further include a photoactive junction. In one embodiment, the layers are epitaxially grown, meaning that they replicate the single crystalline structure of material. The growth parameters (deposition temperature, growth rate, compound alloy composition, and impurity dopant concentrations) are preferably optimized to provide layers with the desired electrical qualities and thickness, to thereby obtain the required overall cell performance. The epitaxial techniques which may be used to grow the cell layers include, by way of example, MOCVD (metal-organic chemical vapor deposition) epitaxy,

sometimes called OMVPE (organic-metallic vapor phase epitaxy), MBE (molecular beam epitaxy), and MOMBE (metal-organic molecular beam epitaxy).

In the illustrated embodiment, an N doped GaAs base layer 106 is grown over and overlays at least a portion of the substrate 102. At the interface between layer 102 and layer 106 a photoactive junction is formed. In one embodiment, the photoactive junction is an N+GaAs/N+Ge heterodiode. In another embodiment, if an N/P configuration is to be grown, a P-type Ge substrate 102 is used, and diffusion of As from the layer 106 forms an N/P junction in the substrate 102.

As illustrated in Figure 1, a highly P doped GaAs emitter layer 108 is grown over at least a portion of the GaAs base layer 106. The base layer 106 and the emitter layer 108 together form a lower cell stage. A highly P doped AlGaAs window layer 110 overlays the emitter layer 108. A tunnel diode, including very highly doped P and N layers 112, 114 is grown over the window layer 110. A second, or upper cell stage, including an N doped base layer 116 and a highly P doped emitter layer 118, is formed over the tunnel diode.

In one embodiment, the last two layers grown for the solar cell are respectively a highly P doped AlGaAs window 120, which is a thin, transparent layer that passivates (reduces carrier recombination) the surface of the emitter layer 118 of the top cell ( $\text{GaInP}_2$ ), and a GaAs cap-layer 122 onto which the front surface ohmic contacts are deposited. In one embodiment, the contacts are in grid-finger form, to balance low electrical resistance and high optical transparency. However, other contact patterns may be used as well. In the present embodiment, as described below, the integral bypass diode is included in the monolithically-grown cell structure by the growth of several additional layers. The cap layer 122 is selectively removed between the gridlines, and anti-reflective coatings are deposited over the top window layer 120.

It will be understood by one of ordinary skill in the art, that the three cell, three-junction, solar cell 100, illustrated in Figure 1, is only one of many possible cell embodiments which can be used with the present invention. In another embodiment, a complementary structure, with the polarities of one or more layers switched (i.e. N doped layers are, instead, P doped, and P doped layers are, instead, N doped), may be used. For example, the cell and diode configurations illustrated in the figures and discussed below, can be changed from P/N to N/P. Also, the doping concentrations or layer thicknesses may be varied. Furthermore, in other embodiments, the solar cell 100 may include four or more photovoltaic cells, or only one or two cells. Similarly, the solar cell may alternatively include only one junction or two or more junctions. By way of example, in one embodiment, the cell 100 may include four junctions.

Furthermore, the solar cell 100 may include cells made from other materials, such as AlGaAs or InP. In other embodiments, the substrate 102 may be formed using a variety of different materials. For example, the solar cell 100 may use other semiconductors, such as GaAs, Si, or InP for the substrate, rather than the Ge substrate 102 illustrated in Figure 1. Alternatively, insulating substrates, such as sapphire, may be used. In one embodiment, the substrate 102 is a single crystal. If the solar cell 100 is intended for space use, such as on a space vehicle or satellite, then the cell materials are preferably space-qualified for the appropriate space environment. For example, the solar cell 100 and bypass diode may be space qualified to operate in an AMD radiation environment.

One method of fabricating the bypass diode will now be described. As illustrated in Figure 2, the bypass diode 212 is included in the solar cell structure using additional five grown layers 202, 204, 206, 208, 210.

As previously described, in one embodiment, the layers 106-122, comprising the photovoltaic portions of the multijunction solar cell 100, are first grown, and the growth cycle is continued to grow the additional layers 202-210.

5 From the P-type GaAs cap layer 122 used for front grid contacts, the additional layers in order are:

- the highly doped N-GaAs connecting layer 202 used to reduce contact resistance to the N-GaAs diode layer 206 and to the highly doped GaAs cap layer 122.
- the stop-etch layer 204 (highly N-doped AlGaAs or GaInP) used to allow controlled etch-removal of the three diode layers 206-210.
- 10 ■ the N doped GaAs layer 206, comprising the negatively doped part of the bypass diode 212.
- the P doped GaAs layer 208, comprising the positively doped part of the of the bypass diode 212.
- the highly doped P-GaAs cap layer 210, used to provide good metallic contact to the P-layer 208 of the diode 212.

15 However, as will be appreciated by one of ordinary skill in the art, other embodiments of the present invention may utilize a different number of layers, formed from different types of materials, and having different dopants than the embodiment described above. For example, the use of the complementary structure, that is, N/P rather than P/N, can similarly consist of N/P multijunction solar cells, and an N/P bypass diode. Also, the diode 212 may be formed using lower bandgap materials, such as germanium or InGaAs. In another embodiment, the layer 202  
20 may be omitted, leaving the layer 204 to provide stop-etching and electrical conduction.

A description of one method of processing a wafer to form one embodiment of the invention will now be described. In the present embodiment, the process steps are used to grow, define by mesa etch, and interconnect one embodiment of the bypass diode 212 into the cascade (multijunction) cell 100.

First, the photoactive solar cell layers and the diode layers illustrated in Figure 2 are epitaxially grown using  
25 conventional MOCVD and/or MBE technologies. As illustrated in Figure 3, the front surface of the grown layer sequence is protected with a photoresist layer 302, which is exposed through a photomask (not shown) patterned to leave the diode layers covered with resist. As illustrated in Figure 4, the diode cap layer 210 and the N and P diode layers 206, 208 are etched down to the stop-etch layer 204. The etching may be performed using citric acid heated to 45°C. As illustrated in Figure 5, the stop etch layer 204 is removed where the photoresist layer 302 does not mask,  
30 and appropriate portions of the N doped GaAs connecting layer 202 is exposed. If the stop etch layer 204 is AlGaAs, then in one embodiment, the etchant may be BHF (buffered hydrofluoric) acid. If the stop etch layer 204 is GaInP, then in another embodiment, the etchant may be HCL. As illustrated in Figure 6, the photoresist layer 302 is removed using acetone. Microstripping techniques may be used to remove any residual photoresist left remaining after the acetone removal process.

Once the photoresist layer 302 is removed, the front contact fabrication process, including corresponding photoresist coating, baking, exposing, developing, metal evaporation, and lift off operations, can take place. Another photoresist layer (not shown) is coated over the whole surface. The photoresist layer is then baked and exposed with a photomask which leaves opened areas where contacts are to be deposited to the front surface gridlines and pads, to a small region of the exposed N doped GaAs layer 202, and to the diode cap layer 210. Metals, predominantly including Ag, are evaporated into the exposed areas and over the remaining photoresist layer. In addition to the two contact areas 702, 704 illustrated in Figure 7, the photoresist also provides open slots in the photoresist, to provide gridlines, and bars/pad contacts to the cell. Next, a lift-off process is performed. The solar cell slice 100 is immersed in acetone, causing the photoresist to swell, and thereby breaks the metal film everywhere except on the regions designated to retain contacts, including contacts 702, 704.

As illustrated in Figure 8, metals, predominantly including Ag, are evaporated over the back surface of the Ge substrate 102 to form a back metal contact 802. The contacts 702, 704, 802 are then heat-treated or sintered. Using the front contact metals 702, 704 as etch-masks, the GaAs cap layer 122 is etched off the major part of the exposed front surface, as illustrated in Figure 9. The cap layer 122 remains under the metallized areas, forming part of a low resistance contact mechanism.

As illustrated in Figure 10, the diode pad metal contacts 702, 704, and the small contacts shown around the diode 212 are protected with a resist mask, and on the rest of the surface, an anti-reflecting layer 1002 is deposited. As illustrated in Figure 11, the top, P-side, diode contact 702 is connected to the back cell (N-grid) contact 802 by bonding a thin interconnect 1102. Thus, in one embodiment, the electrical connection between the P-layer 208 of the P/N GaAs diode 212 and the backside of the N doped Ge substrate 102 is formed by a C-clamp 1102, which is bonded to both the front diode contact 702 and the rear Ge contact 802. Thus, the bypass diode 212 is connected across both of the photovoltaic cells. In other embodiments, the bypass diode may be used to bypass one or more photovoltaic cells. Thus, one embodiment of the present invention can be used to bypass all the cells in a solar cell structure 100, or less than all the cells in the solar cell structure 100.

A variety of other interconnect techniques may be used to connect the solar cell to the bypass diode. The final choice may depend on the additional complexity and the effect on cell yields and costs which results from the use of these alternative approaches. By way of example, descriptions of several other follow.

As illustrated in Figure 12, in one embodiment, a short contact between the diode top contact and a metallized area on a small trough etched down through the cascade cell layers 1206-1218 to expose the Ge substrate 1204 may be used, rather than a C-clamp. The trough may remove less than 1% of the active cell area, and may be located close to the top contact of the bypass diode. As in the previous embodiment, the embodiment illustrated in Figure 12 includes a front metal contact 1224, a rear metal contact 1202, and an anti-reflective coating 1226. Several different contact configurations may be used. By way of example:

- a) In one embodiment (not shown), a short discrete metal interconnect is bonded to the diode contact at one end, and is bonded directly to the Ge surface exposed in the trough. Preferably, the interconnect is gold-plated. A variety



of techniques may be used to make the bond. In one embodiment, the bond is made using eutectic Au-Ge soldering.

- b) If (a), direct bonding to the Ge surface is difficult or undesirable, then, in another embodiment, an additional step may be added to the normal cell processing. The front surface is masked at substantially all regions except where the Ge contact area is needed using dry film or liquid photoresist. Then, when the front metal contacts are deposited through another photoresist mask to form the grid, ohmic and diode contacts, the edges of the trough may be protected with resist by using an opened area just inside the etched area. The metal for contacting the N-Ge may be deposited in the same or a similar deposition sequence as when the front contacts to the cascade cell 100 and the diode contacts 702, 704 are formed. In the present case, TiAuAg or equivalent contacts may serve for the exposed areas on the front surface. A short discrete metal interconnect is bonded to the diode P-contact and the contact to the N-Ge.
- c) As illustrated in Figure 12, in a fully monolithic structure, a trough or recess is etched to the Ge interface 1204 through the diode and cell layers 1206-1218. Thus, the wall or walls of the trough are formed by the cell layers. A mask is then used to expose the edges of the trough, and an insulating layer 1220 is deposited on the layer edges and on the area between the diode cap layer 1218 and the trough. Another mask, which can be included in the main front contact mask, is used to deposit metal 1222, which connects the front contact of the diode to the trough exposing the Ge substrate 1204. In another embodiment, no diode contacts are necessary for the substrate-to-diode interconnect 1222.

Figure 13A illustrates a perspective view of one embodiment of the solar cell 100, including the bypass diode circuit 212. The front surface of the solar cell 100 includes grid lines 1302 interconnected by an ohmic bar 1306. The bar 1306 is shaped to provide an area or recess where the diode 212 is formed. In one embodiment, the diode 212 is interconnected to the back contact 802 of the solar cell 100 using the C-clamp connector 1102 illustrated in Figure 11. Figure 13B illustrates in greater detail the bypass diode 212 illustrated in Figure 13A. In one embodiment, the sides of the diode 212 are interdigitated with the ohmic bar 1306. Thus, the distance between the diode 212 and the bar 1306 is reduced, and more of the bar 1306 is in proximity with the diode 212.

As illustrated in Figure 13A, in one embodiment, three tabs 1304 are mounted on the solar cell 100 for interconnection to an adjoining assembly. The tabs 1304 may include a U-shaped stress relief section, also called a Z-tab. A first side of each of the tabs 1304 is connected to an anode of the cell 100. The solar cell 100 may be interconnected to a second solar cell by connecting a second side of the tabs 1304 to a cathode of the second solar cell. In one embodiment, the tabs are formed from silver, silver-Invar, or silver-clad moly materials.

A coverglass (not shown) may be used to protect the solar cell/bypass diode device. For space applications, the coverglass may be composed of ceria-doped borosilicate coverglass. In one embodiment, the coverglass may have a thickness around 50  $\mu\text{m}$  to 200  $\mu\text{m}$ . The ceria-doped coverglass provides radiation resistant shielding for charged and uncharged particles. In one embodiment, the coverglass will remain substantially transparent when exposed to an AMO space radiation environment spectrum (the spectrum found at Earth's orbit around the sun, outside of Earth's

atmosphere). A major advantage of one embodiment of the integral bypass diode is that the diode does not extend above the front surface of the solar cell 100, and therefore does not require the use of a notched or slotted coverglass to accommodate the integral diode. However, in another embodiment, the integral diode may extend above the front or top surface of the solar cell 100. One skilled in the art will understand that other suitable coverglass materials and dimensions can be used as well.

Figure 14A illustrates still another embodiment of the present invention. The illustrated solar cell 1400 includes a novel buried protective bypass diode 1410. As with the bypass diode 212, the protective bypass diode 1410 is used to protect the solar cell from reverse bias conditions which can result from the shadowing of the cell.

The exemplary grown layer sequence illustrated in Figure 14A is similar to that of Figure 1A. Two additional buried layers 1406, 1408 are provided for polarity matching with the Ge+ emitter 1404. The solar cell 1400 includes a Ge substrate 1402 over which the Ge emitter layer 1404 is grown. Isolated diode layers 1412-1420 form a portion of the bypass diode function. Layers 1422, 1424 form the conventional top cell, over which is a window layer 1426, and a cap layer 1428. In another embodiment, a complementary structure, with the polarities of one or more layers switched from those illustrated in Figure 14A (i.e. P doped layers are, instead, N doped, and N doped layers are, instead, P doped), may be used.

As similarly described above, the solar cell is processed, and, as illustrated in Figure 14B, a back metal contact 1430 and a front metal diode contact 1440 are formed. In addition, an anti-reflective coating 1432 is applied.

In one embodiment, a short integral connector 1436 is formed over an insulator 1434 from the cap layer 1428 on a small trough 1438 etched down through the cell layers 1420-1412 to the tunnel diode layer 1408. An interconnect, such as a C-clamp 1442, may then be used to connect the front metal contact 1440 and the back metal contact 1430. Thus, the bypass diode 1410 is connected in an anti-parallel configuration with respect to the photovoltaic portions of the solar cell 1400 and thereby is configured to provide reverse bias protection to the photovoltaic portions of the solar cell 1400.

Using at least some of the techniques described above, a solar cell incorporating an integral diode onto cascaded cells has achieved efficiencies of well over 21%, and even over 23.5%. These efficiencies are comparable to conventional cascade cells lacking the integral bypass diode. In one embodiment, the integral bypass diode has a forward bias voltage drop of approximately 1.4 to 1.8 volts when conducting 400 mA of forward current. The reverse breakdown voltage is sufficient to block current passing into the bypass diode when the solar cell is forward biased during normal, unshadowed, illumination. In one embodiment, the reverse breakdown voltage is greater than 2.5V.

Furthermore, samples of one embodiment of the present invention, with cell areas of approximately 24 cm<sup>2</sup>, have sustained repeated 10-second pulses of 400 mA of reverse current with no significant change in performance. Thus, for example, when one batch of solar cells incorporating one embodiment of the integral diode were subjected to 2500 pulses of 400 mA reverse current, the following performance changes were observed:

<i>Parameter</i>	<i>Pre-test Measurement</i>	<i>Post-test Measurement</i>
VOC (OPEN CIRCUIT VOLTAGE)	2476 mV	2476 mV
ISC (SHORT CIRCUIT CURRENT)	360.5 mA	359.0 mA
CFF (CURVE FIELD FACTOR)	81.5%	81.5%
Efficiency	22.1%	22%

In other testing, when a reverse current greater in magnitude than ISC passed through the solar cell 100, the area around the diode showed an increase in temperature of only 10-12°C. This small increase in temperature does not have an appreciable affect, either on the performance of the photovoltaic portions of the cell, or on the integral diode.

In another preferred embodiment, the solar cell design described above is modified to even further facilitate its use in either space-based or terrestrial-based concentrator systems. Just as in non-concentrator systems, there is a need to protect against shadowing of the solar cells from clouds, birds, buildings, antennas, or other structures. Thus, protective diodes are still used to protect solar cells from reverse bias conditions resulting from shadowing. However, solar cells in concentrator assemblies typically generate much more power than non-concentrator solar cells. Thus, the protective diodes need to be capable of dissipating heat associated with the much greater power that is bypassed.

In one embodiment, distributing multiple separated bypass integral diodes across at least a portion of the surface of the solar cell helps distribute the heat dissipation. Thus, each of the multiple integral diodes bypasses a portion of the reverse bias power, and correspondingly dissipates a portion of the associated heat. Thus, a single integral diode does not have to bypass all the reverse bias power or dissipate all the heat associated with such bypass function. The multiple integral bypass diodes may be formed using the same technique described above with regard to forming one integral diode. In one embodiment, different photomasks are used to form the diodes and diode contacts.

Figure 15A illustrates one method of interconnecting in series solar cells having integral bypass diodes. By way of example, two solar cells 1502, 1510, with corresponding integral bypass diodes 1504, 1514, are interconnected to form a solar cell string 1500. A first interconnect 1508 is connected to a front contact 1506, overlaying cascaded cells of the solar cell 1502, and to a front contact 1512, overlaying the integral bypass diode 1514 of the solar cell 1510, thereby electrically coupling the solar cells 1502, 1510. The first interconnect 1508 may be a jumper bar, wire, or the like. A second interconnect 1518 is connected to the front contact 1506 of the solar cell 1502, and to a back contact 1516 of the solar cell 1510. The second interconnect 1518 may be a z-tab, wire, or the like. In the illustrated embodiment, the bypass diodes 1504, 1514 are conveniently located on the edge or side opposite the Ohmic cell contact pads 1506, 1520.

Figure 15B illustrates another method of interconnecting in series solar cells having integral bypass diodes. As in the previous example, the first interconnect 1508 is connected to the front contact 1506 of the solar cell 1502, and to the front contact 1512 of the solar cell 1510. The second interconnect 1518 is connected to the front contact

1512 and to the back contact 1516 of the solar cell 1510. The second interconnect 1518 may be a C-clamp, wire, or the like. This embodiment can advantageously use only one interconnect between two adjacent cells, and the series connection between the cells can be made on the front surfaces of the cells. Thus, by way of example, the cells can first have their corresponding C-clamps individually affixed by the cell manufacturer. The solar cell panel assembler  
5 can then appropriately position the cells in long strings, and then interconnect the front contacts of the cells as illustrated in Figure 15B. This procedure can provide for the efficient, high yield manufacture of solar cells, solar cell strings, and solar cell panels.

While certain preferred embodiments of the invention have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the present invention.

## WHAT IS CLAIMED IS:

1. A protected solar cell circuit comprising:
  - a first photovoltaic cell;
  - a first contact coupled to said first photovoltaic cell;
  - a second photovoltaic cell overlaying at least a portion of said first photovoltaic cell;
  - 5 a cap layer overlaying at least a portion of said second photovoltaic cell;
  - an epitaxially grown diode overlaying at least a portion of said cap layer;
  - a second contact formed on at least a portion of said cap layer;
  - a first conductor electrically coupling said diode to said first contact; and
  - a second conductor electrically coupling said bypass diode to said second contact so that said diode
  - 10 acts as a bypass diode for said first and said second photovoltaic cells.
2. The protected solar cell circuit as defined in Claim 1, wherein said solar cell circuit is formed from at least Group III and Group V elements.
3. The protected solar cell circuit as defined in Claim 1, further comprising a window layer located between said cap layer and said second photovoltaic cell.
- 15 4. The protected solar cell circuit as defined in Claim 1, further comprising a germanium substrate.
5. The protected solar cell circuit as defined in Claim 1, further comprising a GaAs substrate.
6. The protected solar cell circuit as defined in Claim 1, further comprising an insulating substrate.
7. The protected solar cell circuit as defined in Claim 1, wherein said bypass diode is space qualified to operate in an AMO environment.
- 20 8. A solar cell circuit comprising:
  - a multijunction solar cell device having at least two photovoltaic cells; and
  - a first bypass diode epitaxially grown on said multijunction solar cell portion to protect at least a first and a second of said at least two photovoltaic cells.
9. The solar cell circuit as defined in Claim 8, wherein said multijunction solar cell portion includes at least a first cell and a second cell and said first bypass diode portion includes a first contact and a second contact.
- 25 10. The solar cell circuit as defined in Claim 9, further comprising:
  - a third contact coupled to said first cell;
  - a cap layer overlaying at least a portion of said second cell;
  - a fourth contact coupled to said cap layer;
  - 30 a first conductor coupling first contact to said third contact; and
  - a second conductor coupling said second contact to said fourth contact.
11. The solar cell circuit as defined in Claim 10, wherein said fourth contact is located at the bottom of a recessed region.

12. The solar cell circuit as defined in Claim 11, further comprising a substrate, wherein recessed region extends down to said substrate.

13. The solar cell circuit as defined in Claim 11, further comprising at least a second diode portion.

14. The solar cell circuit as defined in Claim 11, wherein formation of said recessed region reduces the active cell area by less than 1%.

15. The solar cell circuit as defined in Claim 10, wherein said first conductor is a monolithic conductor.

16. The solar cell circuit as defined in Claim 10, wherein said first conductor is a discrete metal interconnect.

17. The solar cell circuit as defined in Claim 10, wherein said first conductor is a C-clamp metal interconnect.

18. A solar cell device comprising:

a GaAs-type cell;

a first contact coupled to said GaAs-type cell;

a tunnel diode overlaying at least a portion of said GaAs-type cell;

15 a GaInP-type cell overlaying at least a portion of said tunnel diode;

a cap overlaying at least a portion of said GaInP-type cell;

a second contact overlaying at least a portion of said cap;

an epitaxially grown bypass diode overlaying at least a portion of said cap;

a third contact coupled to said bypass diode;

20 a fourth contact coupled to said bypass diode;

a first conductor which couples said second contact and said third contact; and

a second conductor which couples said first contact and said fourth contact.

19. A solar cell device comprising:

a first cell;

25 a first contact coupled to said first cell;

a second cell overlaying at least a portion of said first cell;

a second contact coupled to said second cell;

an epitaxially grown diode overlaying at least a portion of said second cell;

a first conductor electrically coupling said bypass diode to said first contact; and

30 a second conductor electrically coupling said bypass diode to said first contact.

20. A protected solar cell circuit comprising:

a first solar cell portion including at least one junction and at least one solar cell contact on a backside of said first solar cell portion;

35 at least one bypass diode portion epitaxially grown on said first solar cell portion, said bypass diode having at least one contact; and

a discrete interconnect coupling said solar cell contact to said diode contact.

21. A protected solar cell circuit as defined in Claim 20, further comprising a plurality of other solar cell portions coupled in series or in parallel with said first solar cell portion.

22. A spacecraft comprising:

a first solar cell used to power said spacecraft, wherein said first solar cell includes at least:

a cap layer;

a contact formed on said cap layer

an integral bypass diode overlaying at least a portion of said cap layer, said bypass diode having at least one contact; and

an interconnect coupling said cap layer contact to said diode contact; and

a second solar cell used to power said spacecraft, said second solar cell coupled to said first solar cell.

23. A solar cell assembly comprising:

a means for converting solar cell energy into electrical energy, said means for converting solar energy having a plurality of cells;

a means for accepting a contact overlaying at least a portion of said means for converting solar energy;

a contact overlaying at least a portion of said means for accepting a contact; and

a means for protecting said means for converting solar energy from a reversed biased condition,

wherein said means for protecting is coupled to said contact using a means for conducting.

24. A method of fabricating a solar cell circuit, comprising the acts of:

providing a first photovoltaic cell;

providing a second photovoltaic cell coupled to said first photovoltaic cell;

providing a cap layer coupled to said second photovoltaic cell; and

providing an integral bypass diode coupled to said cap layer.

25. A method of fabricating a protected solar cell circuit, comprising the acts of:

growing a first plurality of layers to form at least a part of a multijunction solar cell;

growing a second plurality of layers over at least a portion of said first plurality of layers to form a diode;

etching away at least a portion of said second plurality of layers;

providing a first contact on at least a portion of one of said first plurality of layers;

providing a second contact on at least a portion of one of said second plurality of layers; and

coupling said first contact to said second contact, wherein said diode acts as a bypass diode.

26. The method of fabricating a protected solar cell circuit as defined in Claim 25, wherein said first set of layers includes at least one cap layer.

27. The method of fabricating a protected solar cell circuit as defined in Claim 26, wherein said first contact is positioned at least partly on said cap layer.

28. The method of fabricating a protected solar cell circuit as defined in Claim 25, wherein said first contact is coupled to said second contact using an integral conductor.

5 29. The method of fabricating a protected solar cell circuit as defined in Claim 25, wherein said first contact is coupled to said second contact using a discrete conductor.

30. A protected solar cell circuit comprising:

a substrate;

a first photovoltaic cell coupled to said substrate;

10 a second photovoltaic cell coupled to said first photovoltaic cell;

an epitaxially grown bypass diode coupled to said second photovoltaic cell;

a recessed region having at least one wall defined by at least said first photovoltaic cell, said second photovoltaic cell, and said diode, said recessed region extending from said diode to said substrate;

an insulator deposited on said at least one wall of said recessed region; and

15 a conductive material deposited on at least a portion of said diode and at least a portion of said insulator so as to electrically couple said diode to said substrate.

31. A solar cell circuit comprising:

a first photovoltaic portion;

a substrate; and

20 a diode used to provide reverse bias protection formed between said first photovoltaic portion and said substrate.

32. The solar cell circuit as defined in Claim 31, further comprising a second photovoltaic portion.

33. The solar cell circuit as defined in Claim 31, wherein said first photovoltaic portion has a P/N structure.

25 34. The solar cell circuit as defined in Claim 31, wherein said bypass diode has an N/P structure.

35. The solar cell circuit as defined in Claim 31, wherein said bypass diode has a P/N structure.

36. The solar cell circuit as defined in Claim 31, wherein said first photovoltaic portion has an N/P structure.

37. A method of interconnecting solar cells, comprising:

30 interconnecting a first contact of a first solar cell, said first solar cell having an integral bypass diode, with a first contact of a second solar cell; and

interconnecting said first contact of said first solar cell with a second contact of said second solar cell.

38. The method of interconnecting solar cells as defined in Claim 37, wherein said first contact of said first solar cell is interconnected to said second contact of said second solar cell using a z-tab interconnect.



39. The method of interconnecting solar cells as defined in Claim 37, wherein the integral diode of said first solar cell is spaced away from said first contact in a first direction.

40. A method of interconnecting solar cells, comprising:  
interconnecting a first contact of a first solar cell, said first solar cell having an integral bypass  
5 diode, with a first contact of a second solar cell; and  
interconnecting said first contact of said second solar cell with a second contact of said second solar cell.

41. The method of interconnecting solar cells as defined in Claim 40, wherein said first contact of said second solar cell is interconnected to said second contact of said second solar cell using a C-clamp.

10 42. The method of interconnecting solar cells as defined in Claim 40, wherein said first contact of said first cell is on the front of said first cell, said first contact of said second cell is on the front of said second cell, and said second contact of said second cell is on the back of said second cell.

43. A method of interconnecting solar cells, comprising:  
attaching a conductor to a first contact located on the front of a first solar cell having an integral  
15 bypass diode; and  
attaching said conductor to a second contact located on the front of a second solar cell.

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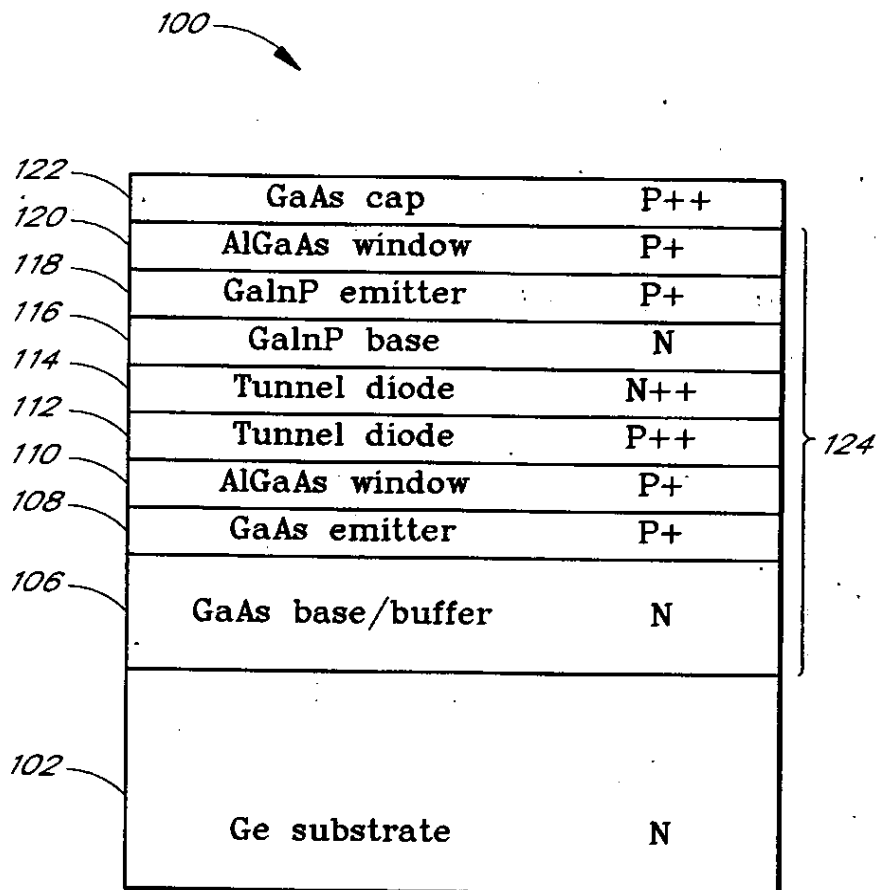


FIG. 1

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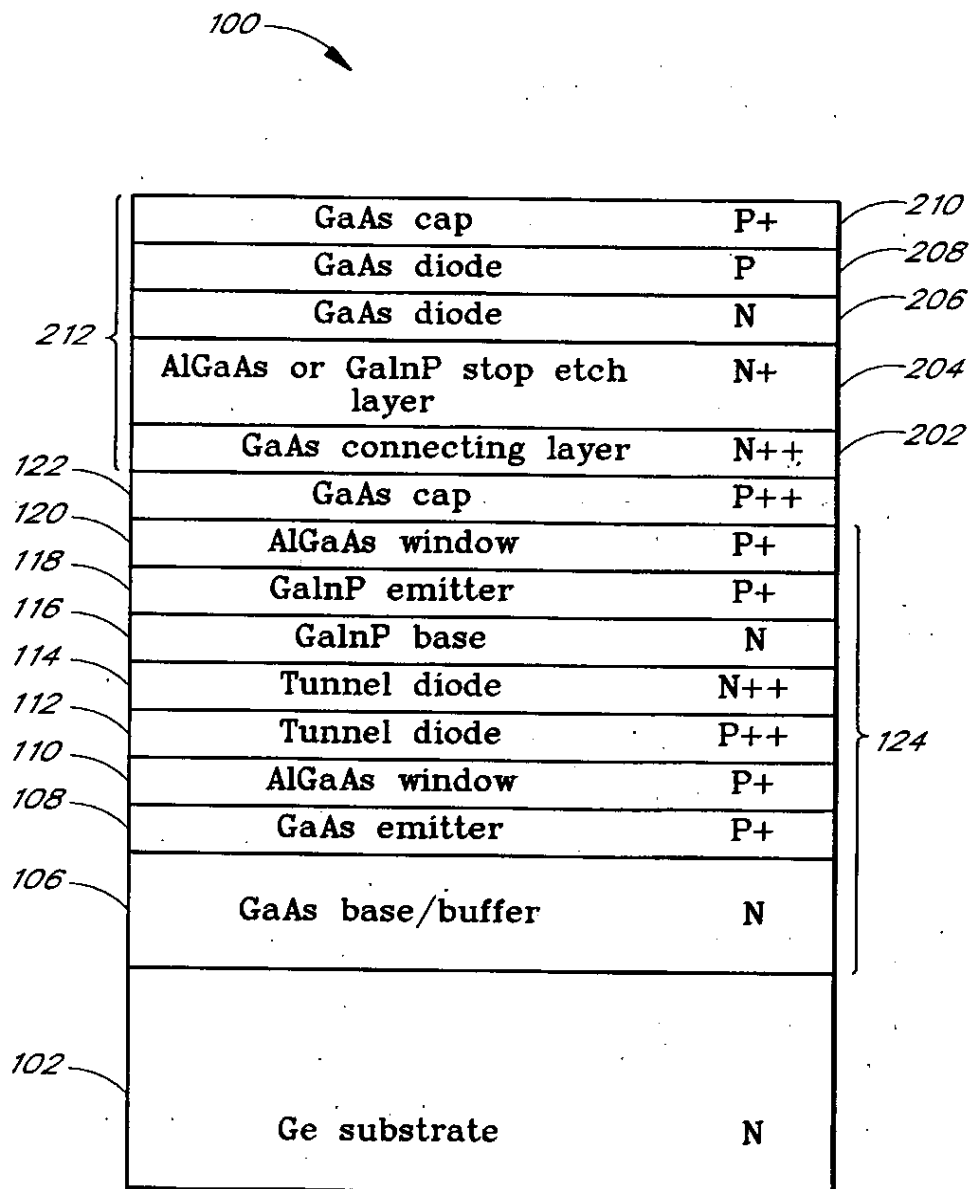


FIG. 2

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302	Photoresist layer
216	Diode Cap Layer P++
208	p- Diode Layer (GaAs)
206	n- Diode layer (GaAs)
204	Stop Etching Layer (AlGaAs or GaInP)
202	GaAs N connecting layer N++
122	GaAs Cap layer P++
124	Cascade Solar Cell P/N
102	Ge Substrate N

FIG. 3

Citric Acid (45° C, 1 min.)

Photoresist layer
Diode Cap Layer P++
p- Diode Layer (GaAs)
n- Diode layer (GaAs)
Stop Etching Layer (AlGaAs or GaInP)
GaAs connecting layer N++
GaAs Cap layer P++
Cascade Solar Cell P/N
Ge Substrate N

FIG. 4

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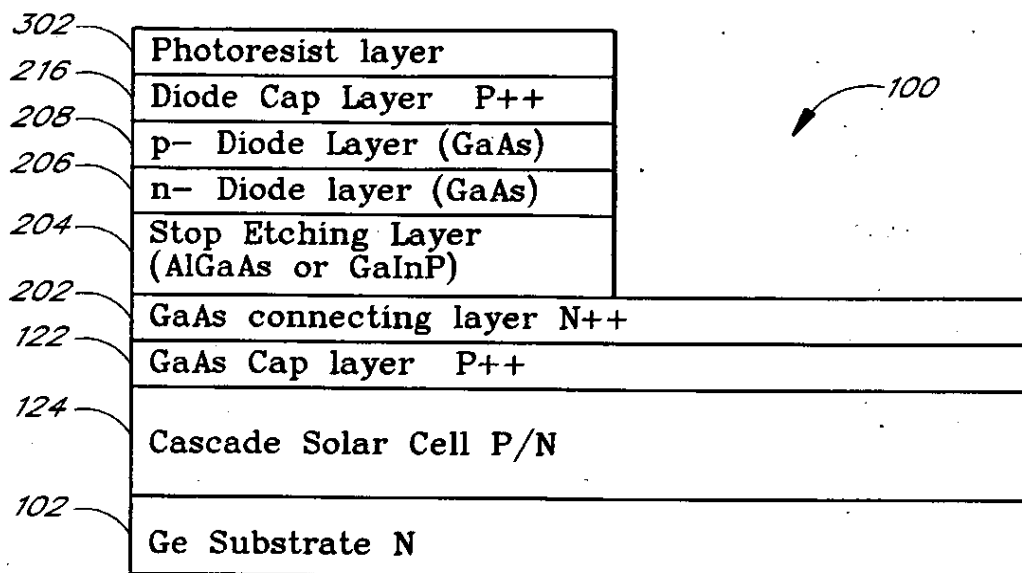


FIG. 5

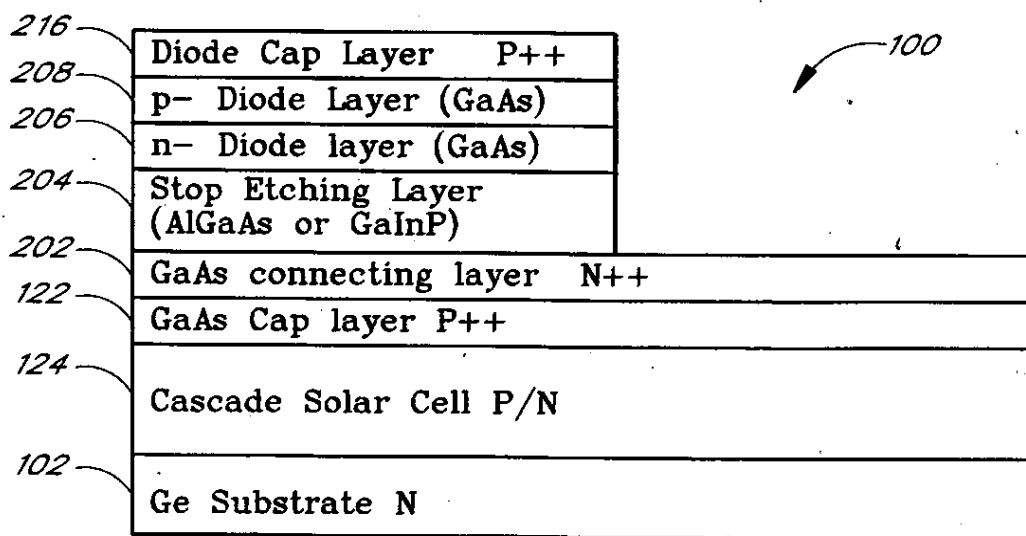


FIG. 6

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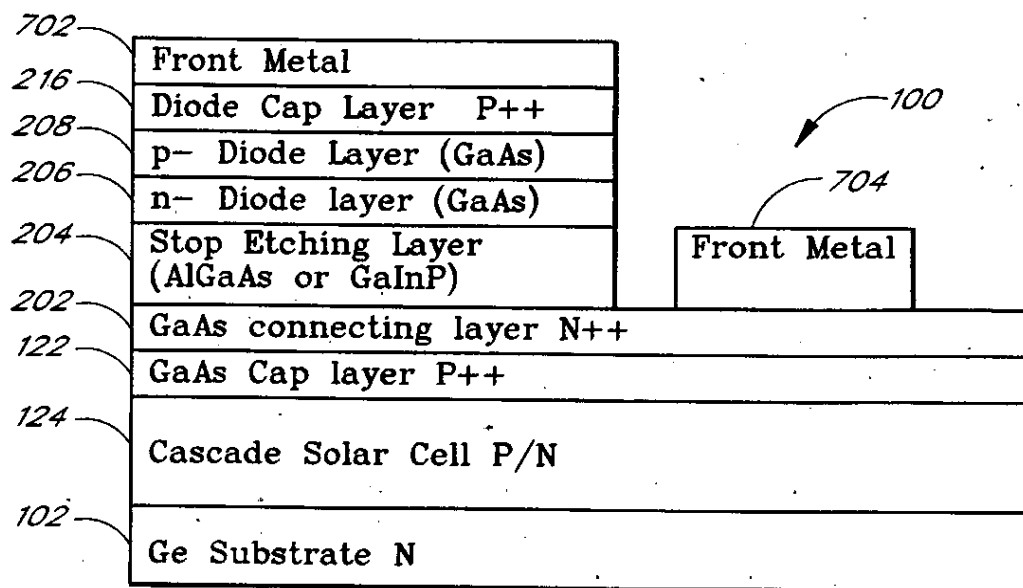


FIG. 7

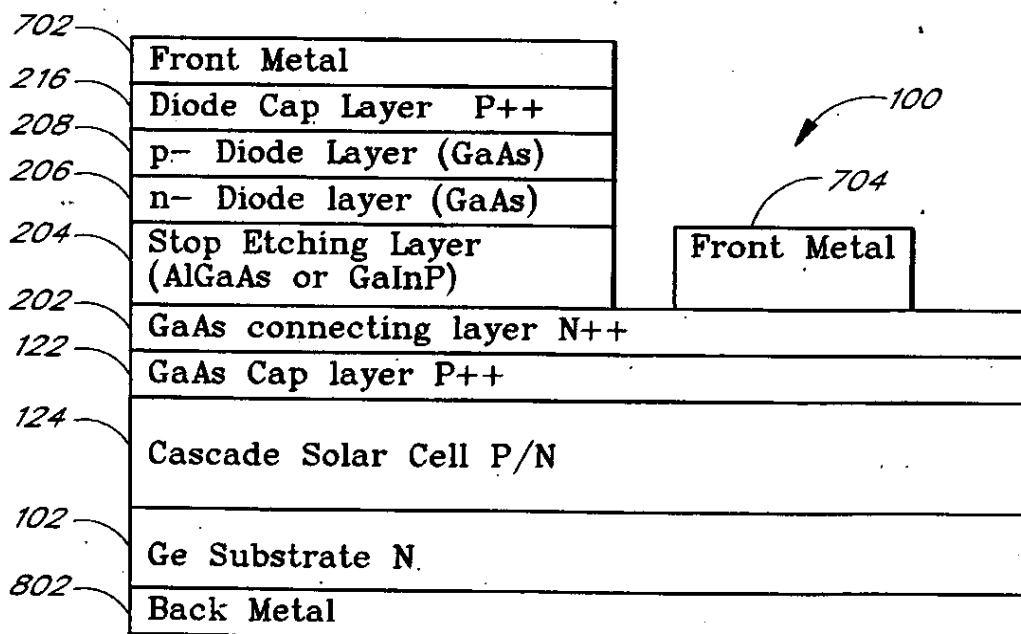


FIG. 8

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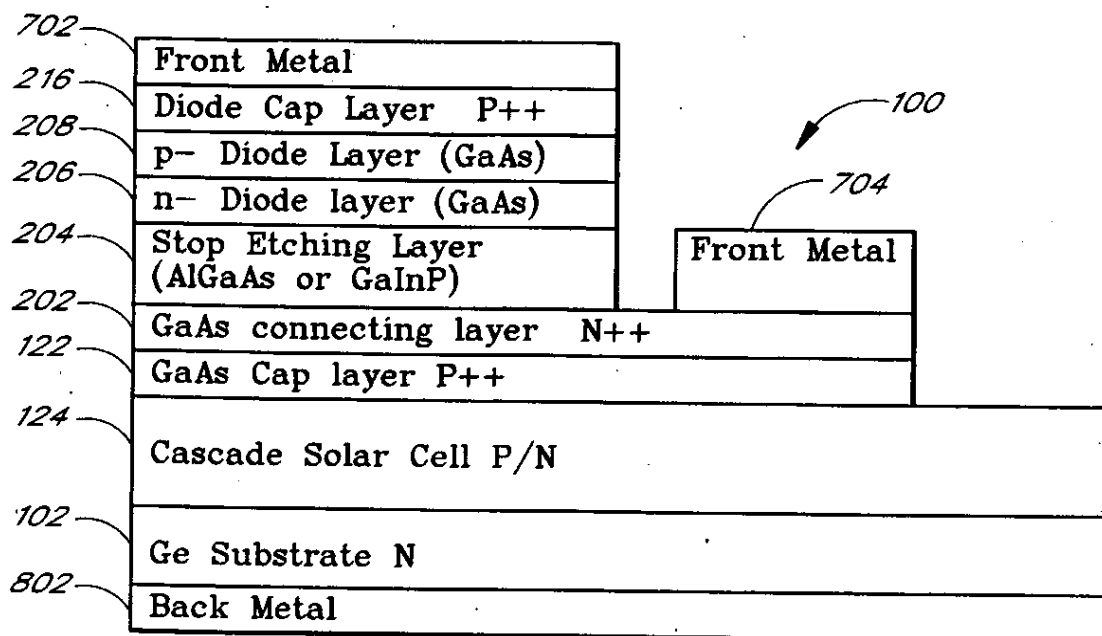


FIG. 9

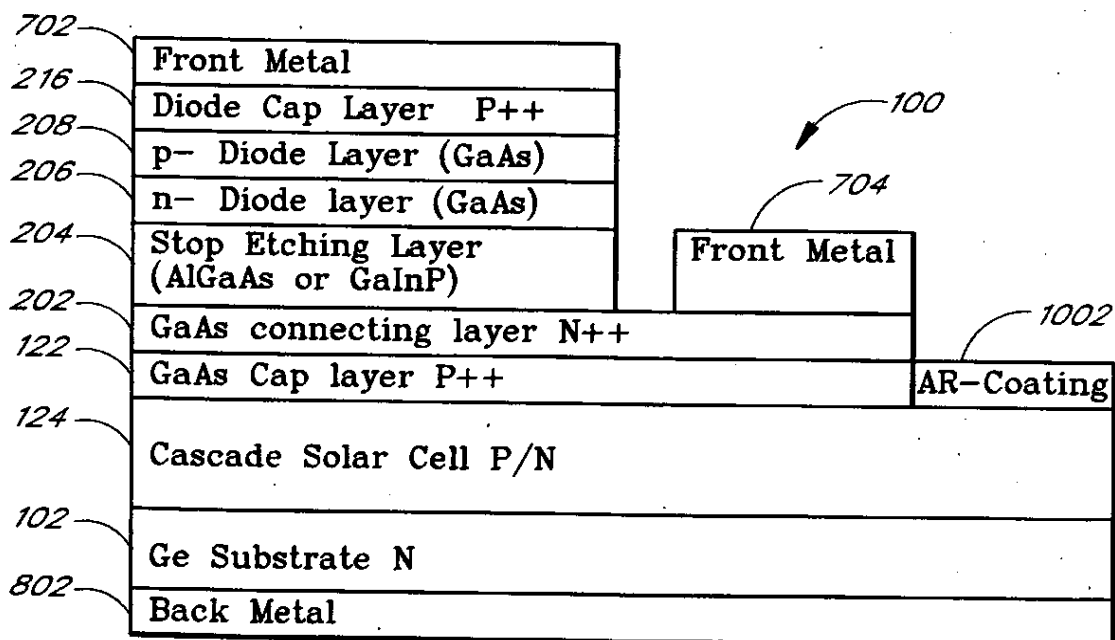


FIG. 10

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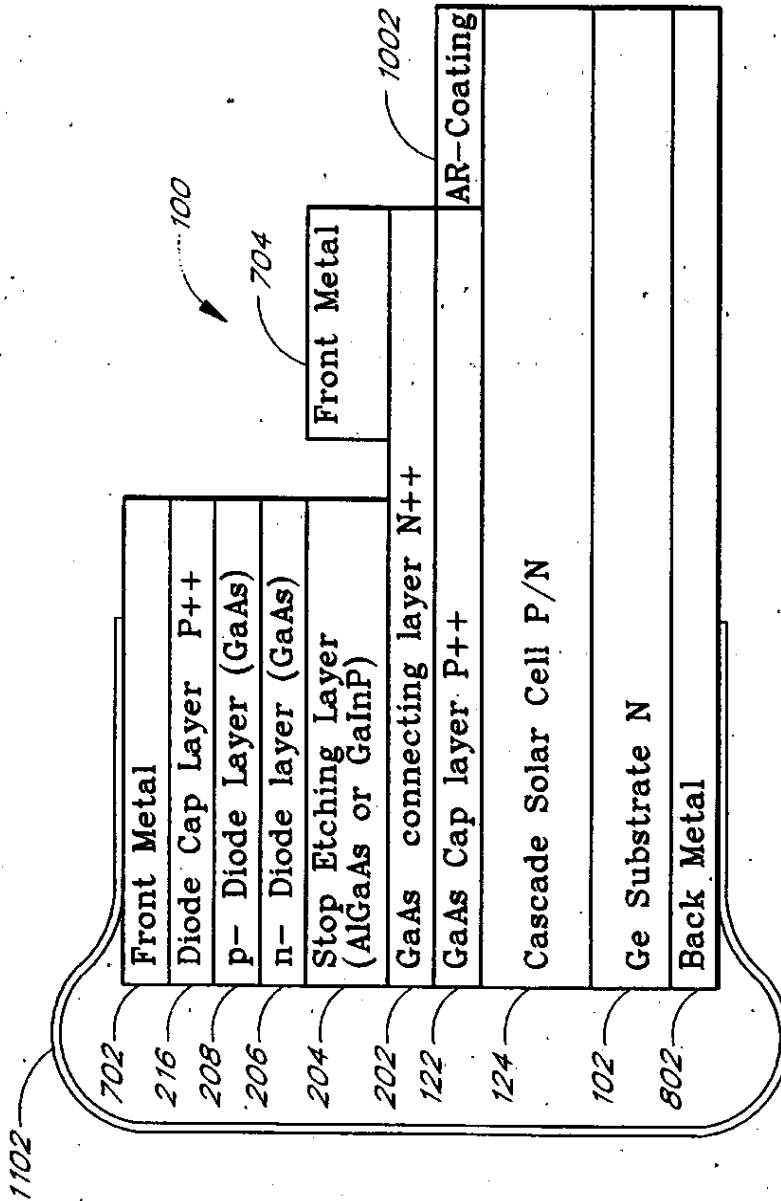


FIG. 11



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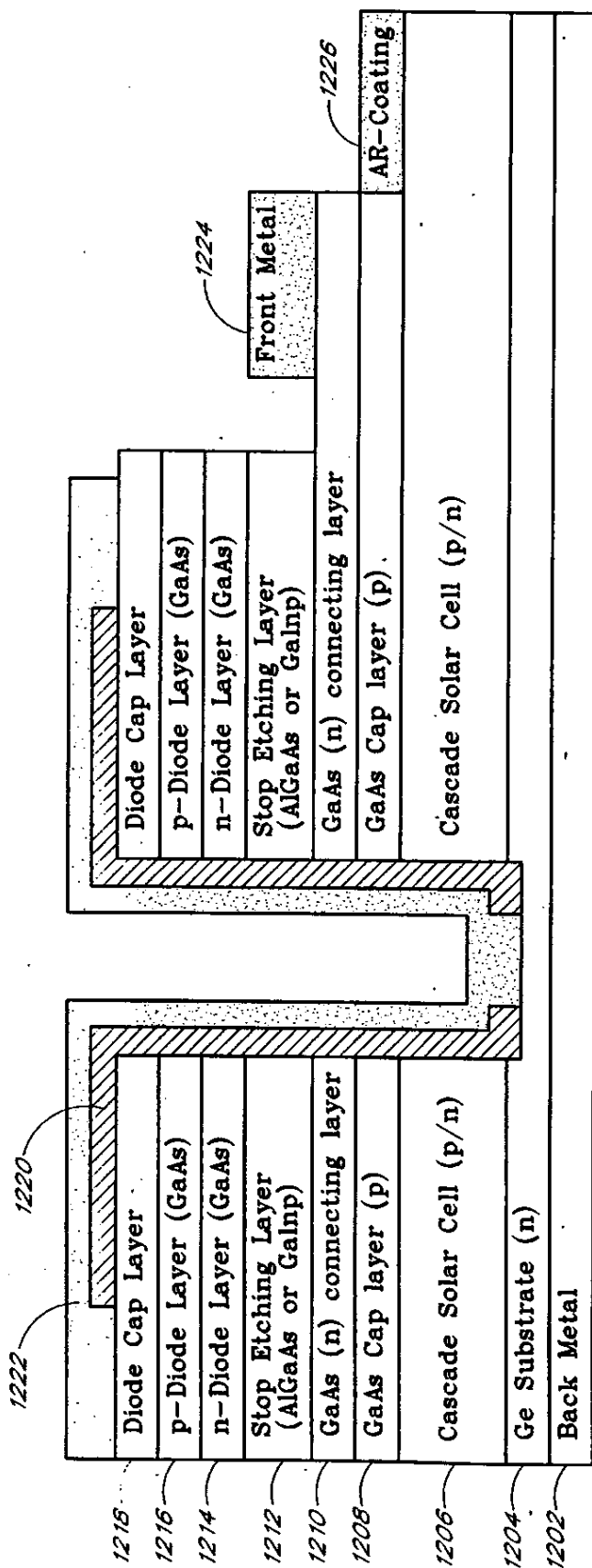


FIG. 12

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FIG. 13A

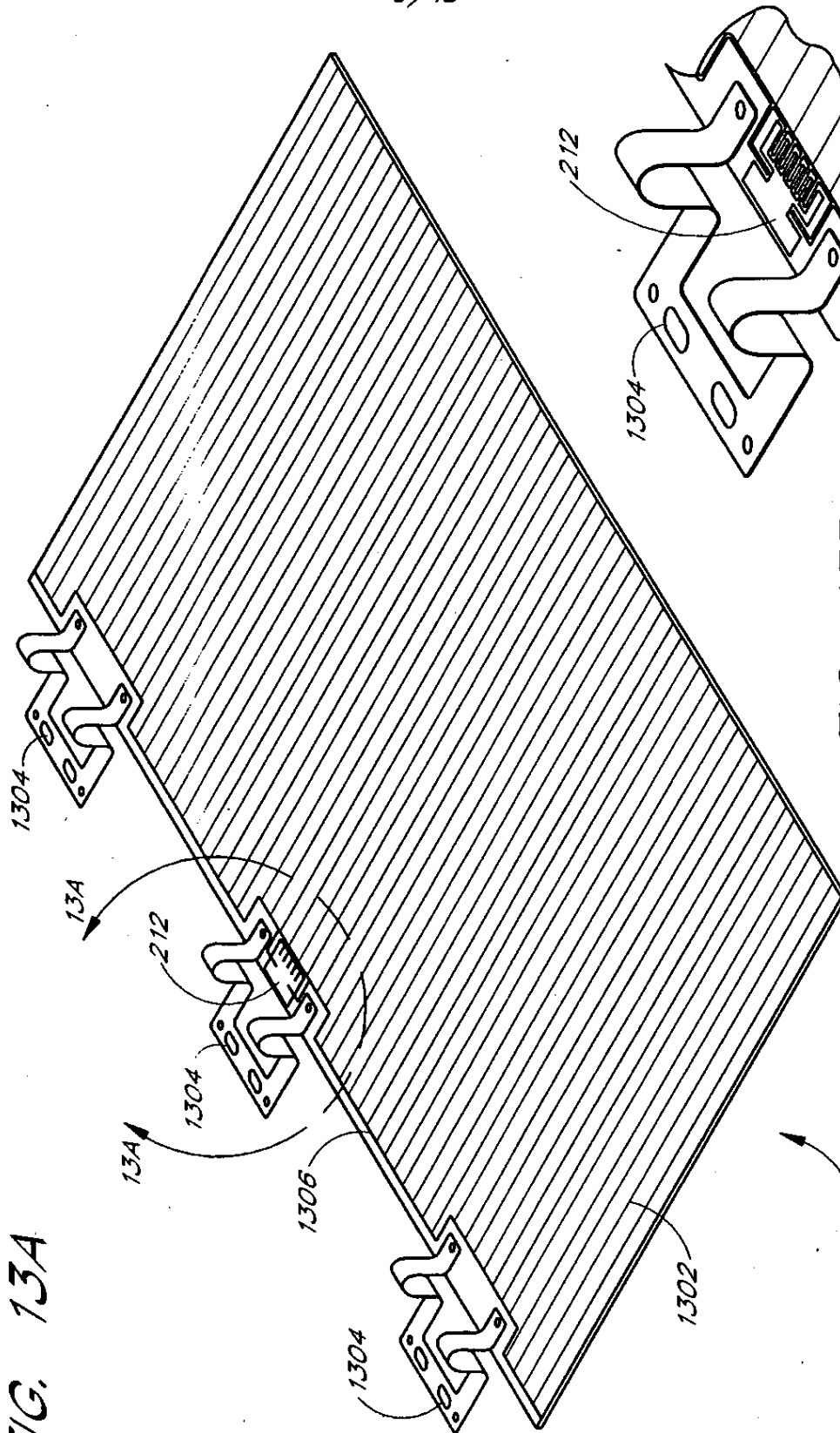
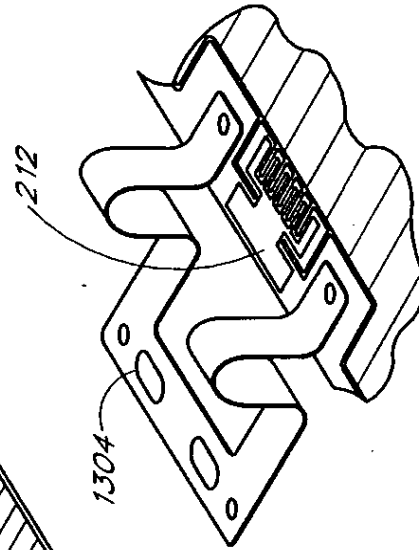


FIG. 13B



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1400

1428	GaAs Cap	P+
1426	AlGaAs Window	P+
1424	GaInP emitter	P+
1422	GaInP Base	N
1420	Tunnel Diode	N++
1418	Tunnel Diode	P++
1416	AlGaAs Window	P+
1414	GaAs emitter	P+
1412	GaAs Base/Buffer	N
1408	Tunnel Diode	N++
1406	Tunnel Diode	P++
1404	Ge emitter	P+
1402	Ge base/substrate	N

1410

FIG. 14A

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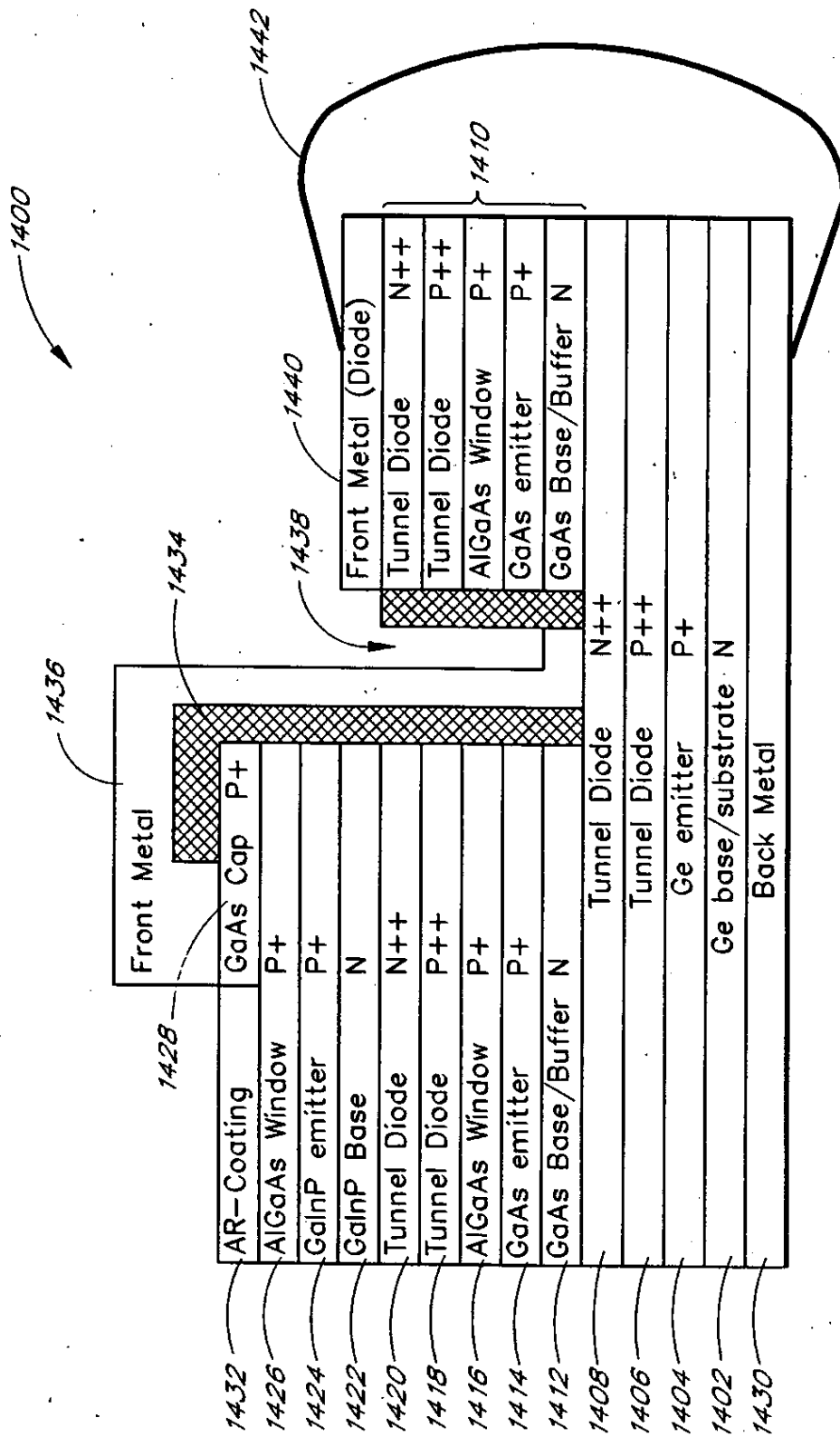


FIG. 14B

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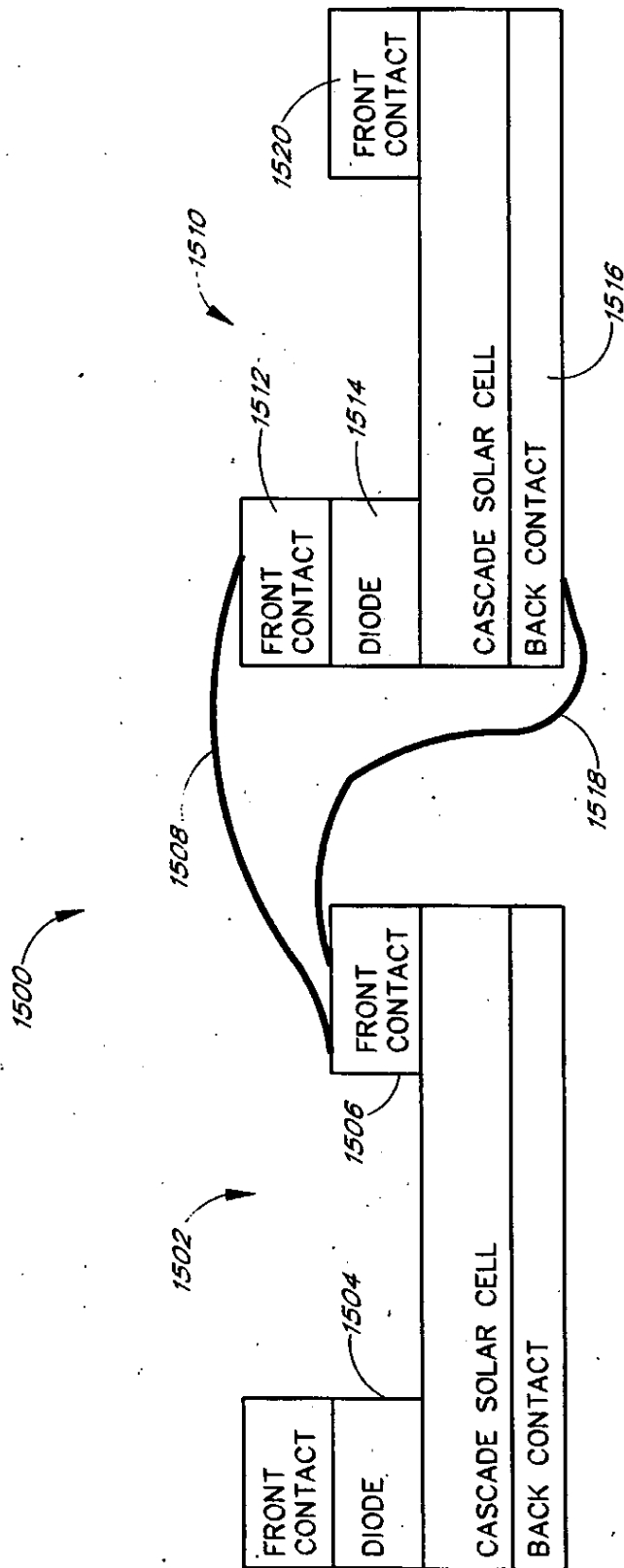


FIG. 15A

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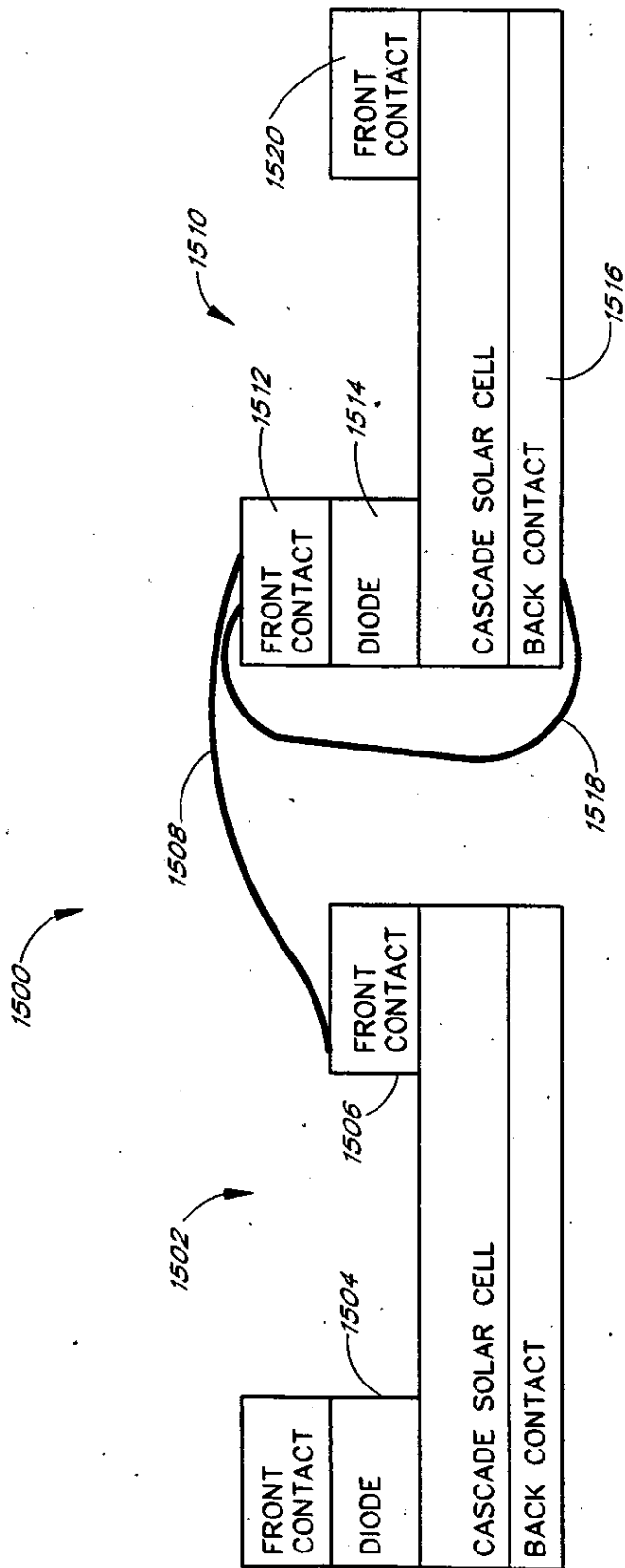


FIG. 15B

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US99/11171

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H01L 31/042, 31/05, 31/06, 31/18, 27/142, 23/62

US CL : Please See Extra Sheet.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 136/244, 249, 255, 256, 262, 252; 257/443, 459, 461, 428, 431; 438/66, 73, 74, 83, 94, 98

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,759,803 A (COHEN) 26 July 1988, col. 3, line 61 through col. 5, line 4.	20-24, 30, 37-43
Y		1-19, 25-29, 31-36
X	US 5,616,185 A (KUKULKA) 01 April 1997, Figure 2 and col. 3, line 54 through col. 4, line 56.	20, 21, 23, 30, 37-43
Y		1-19, 22, 24-29, 31-36
X	WO 96/18213 A1 (GREEN et al) 13 June 1996, Figure 1 and page 7, lines 4-34.	31
Y		1-30, 32-43

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
*A* document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
*E* earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*A* document member of the same patent family
*O* document referring to an oral disclosure, use, exhibition or other means	
*P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

16 JULY 1999

Date of mailing of the international search report

16 SEP 1999

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Box PCT  
Washington, D.C. 20231

Facsimile No. (703) 305-3230

Authorized officer

ALAN D. DIAMOND

Telephone No. (703) 308-0661

## INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US99/11171

## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,330,583 A (ASAI et al) 19 July 1994, col. 6, line 43 through col. 7, line 58.	1-43



INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US99/11171

A. CLASSIFICATION OF SUBJECT MATTER:  
US CL :

136/244, 249, 255, 256, 262, 252; 257/443, 459, 461, 428, 431; 438/66, 73, 74, 83, 94, 98